REMARKS

Applicant concurrently files herewith an Excess Claim Fee Payment Letter for five (5) excess independent claim and three (3) excess total claims.

Claims 1-20 are presently pending in this application. Claims 1, 3, 5-8, and 10-17 have been amended to more particularly define the invention. Claims 19-23 have been added to assure Applicant the degree of protection to which his invention entitles him.

Applicant gratefully acknowledges that claims 1-9 have been allowed and that claims 11 and 17-18 have been indicated to be allowable if rewritten in independent form. However, Applicant respectfully submits that all of the claims are allowable.

It is noted that the claim amendments to claims 1-9, 11, and 17-18 are made only to assure grammatical and idiomatic English and improved form under United States practice, and are not made to distinguish the invention over the prior art or narrow the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any of those claim should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim. The claim amendments include utilizing "said" to refer back to positively recited claim elements, and utilizing "the" to refer back to environmental elements.

Claim 12 was rejected under 35 U.S.C. §112, second paragraph for lack of antecedent. Claim 12 has been amended to correct this. Therefore, this rejection is overcome.

Claims 10 and 13-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yen, U.S. Patent No. 5,272,586. This rejection is respectfully traversed.

The claimed invention of claims 10 and 13-16 is directed to a surge protection circuit. An exemplary embodiment of the invention includes first and second pluralities of pad electrodes, vertical signal lines connected respectively to the first plurality of pad electrodes,

horizontal signal lines intersecting the vertical signal lines and connected respectively to the second plurality of pad electrodes, and a plurality of floating-gate field effect transistors.

Each transistor has a channel capacitance and includes a floating gate electrode, a source electrode, and a drain electrode. The source and drain electrodes of each of the transistors are respectively connected to the drain and source electrodes of adjacent ones of the plurality of floating-gate transistors and are further connected to respective ones of the first plurality of pad electrodes. The transistors are responsive to one of the first plurality of pad electrodes or one of the plurality of vertical signal lines being subjected to a surge potential for developing a voltage on the channel capacitance sufficient to turn on the floating-gate field effect transistor and establish connections with the adjacent floating-gate transistors. This rapidly provides a low impedance path to dissipate the surge voltage.

In a second exemplary embodiment, the source and drain electrodes of each of the transistors are respectively connected to the vertical signal lines. The transistors are responsive to one of the first plurality of pad electrodes or one of the plurality of vertical signal lines being subjected to a surge potential for developing a voltage on the channel capacitance sufficient to turn on the floating-gate field effect transistor and establish a low-impedance path to ground.

Yen discloses a technique for improving electrostatic discharge immunity in an integrated circuit. A switching MOS transistor utilizing floating gate technology is used to shunt electrostatic discharge away from the integrated circuit. However, Yen's transistors have a gate electrode which is connected to either the circuit under protection or to a voltage source. There is no disclosure of a channel capacitance on which a voltage surge develops a voltage sufficient to turn on the floating-gate field effect transistor.

In independent claims 10 and 16, and thus also in dependent claims 13-15, the floating-gate field effect transistors have a channel capacitance, and the transistors are responsive to one of the first plurality of pad electrodes or one of the plurality of vertical signal lines being subjected to a surge potential for developing a voltage on the channel capacitance sufficient to turn on the floating-gate field effect transistor. There is no disclosure or suggestion of this in Yen. It is accordingly submitted that these claims are allowable.

Claims 19-23 have been added to assure Applicant the degree of protection to which his invention entitles him. These claims distinguish from the references just as do claims 1-18, and so are also allowable.

In view of the foregoing, Applicant submits that claims 1-23, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper,

including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

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